Why do the slides look like this?

(New) Faculty Forum - February 5, 2013
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Midterm Exam #1

- Friday, February 8, in class
- “Practical” circuit problems
- “Theory” concept/explanation problems
- Problem sets, Review packages, textbook readings
Recent handouts

• Problem Set #5
• Midterm Exam #1 – Review
• Midterm Exam #1 – Information
• Introduction – Part B
• Review – Part B (website)
New handouts

• Midterm #1 – Review problems
• Problem Set #5
• Problem Set #5 solutions (website)
Problem Set #5

- Handed out today
- Also available on course website
- Problems on $R$-$C$ delay and transistor sizing
Course website

• URL: http://ece304.jsit.ca
• Username: student
• Password: Digital101 (note: case sensitive)
• Please visit often
Summary of last class

- Using the simplified $R$-$C$ model
  - $R$ scales inversely with $W$; $C$ scales directly with $W$
- Replace FETs with $R$-$C$ models
- Simplify the $R$-$C$ circuit
A.5 Pass-transistor logic and trans. gates

• the “bad” non-invertor (buffer)
  • strong vs. degraded 1s and 0s
• the transmission gate
• pass-transistor logic
A.5.3 Pass-transistor logic

• Consider a 2:1 multiplexor

• Write down function $Y = f(S, P, Q)$.

• List all possible functions of one variable $Y = f(S)$. 
Prob A-15: AND gate

Implement an AND gate \( Y = AB \)

a) Implement using fully complementary static CMOS logic. How many transistors are required?

\[ \text{AND} = \text{NOT NAND} \]
b) Use 2:1 multiplexors...
Prob A-15: AND gate

c) Use 2:1 multiplexors...
B.1.4 Transistor sizing

- We want to design logic gates so that their delay is the same or better than the unit width inverter.
- This means the pull-up and pull-down resistance must be $\leq R$ in all cases.
Prob B-4: Complex gate transistor sizing

• Size the transistors appropriately...
B.1.5 Elmore delay

- Approximate the delay of a complex R-C network “tree”.
- Easiest to understand by looking at examples.
B.1.6 Logical effort

• Text:
  • 3rd ed. §4.2~4.3
  • 4th ed. §4.3~4.5

I think I can, I think I can ...